REMARKS/ARGUMENTS

In this amendment, claims 1-2, 4-10, 14, 20-21, 23-29, and 33 are amended. No claims are canceled or added. Thus, claims 1-15, 20-34, 36 and 37 remain pending.

Rejections under 35 USC § 103(a), Leaver in view of Cong

Claims 1-9, 20-28 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. (US Patent No. 6,195,788) in view of Cong et al. ("Cut Ranking and Pruning: Enabling a General and Efficient FPGA Mapping Solution").

Claims 1-15

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *A method of determining an implementation of a user design on a programmable device including a plurality of programmable logic elements, each comprising reconfigurable logic hardware and fixed-configuration secondary hardware ..., the method comprising:*
>
> *for each of a plurality of portions of the user design, determining one or more sets of input assignments to the fixed-configuration secondary hardware, each set providing an implementation of that portion of the user design using the fixed-configuration secondary hardware;*
>
> *ranking the input assignments by determining a number of times each of a plurality of signals in the user design is assigned as a respective input to the fixed-configuration secondary hardware.*

Leaver determines whether a particular logic region (cone) of a user design should be implemented using PTERM or LUT logic elements. *See Leaver*, col. 7 lines 26-29. First, a PTERM mapping and a LUT mapping of the user design is created. *Id.*, col. 7 lines 14-16. Note that a mapping divides a user design into logic cells (e.g. gates and registers) that are mapped onto logic elements of the target device. *Id.,* col. 4 lines 28-41. The mappings are then used to create logic regions (cone) that are generated by choosing two anchors (logic elements that generate the same logic function in either mapping) and by taking the logic between the anchor points as the logic cone. *Id.*, col. 7 lines 44-51 and col. 8 lines 5-25.

At page 2, the Office Action seems to equate the anchors with the fixed-configuration secondary hardware of claim 1. As described above, the anchors are certain functional points in the mapping and are not a particular piece of hardware in the programmable logic device. Thus, the anchors do not teach or suggest the fixed-configuration secondary hardware of programmable logic elements of the programmable device, as recited in claim 1.

Additionally, Leaver mentions that each node (logic element) in the netlist is grouped into a logic cone. *Id.*, col. 9 lines 60-67. This simply states that there is a logic cone for each logic element of a mapping, i.e. all nodes between anchors. *Id.*, Figs. 4A and 4b. However, there is no mention of the anchors in this cited passage, and nowhere does Leaver mention determining input assignments to the anchors. Accordingly, even if the anchors could be construed as the fixed-configuration secondary hardware, Leaver does not teach or suggest "*determining one or more sets of input assignments to the fixed-configuration secondary hardware*."

Furthermore, Leaver's Table 1 shows a comparison of the relative cost of using PTERM logic elements relative to using LUT logic elements for each logic cone. *Id.*, col. 10 lines 1-40. The relative cost is for using a LUT or PTERM for the logic within a logic cone, and not a cost of an assignment of a particular input. Particularly, the anchors are not involved in the relative cost. Accordingly, Leaver does not teach or suggest "*ranking the input assignments*" to the fixed-configuration secondary hardware, as recited in claim 1.

Moreover, Cong does not teach any of the limitations above, alone or in combination with Leaver. The cited passages discuss how to make cuts (similar to logic cones) in the user design. Cong states that the cuts would be done differently if the FPGA had LUTs of different sizes (i.e. heterogeneous). *See Cong,* section 3.3.5. These cuts are performed at a mapping stage, and are then ranked. *Id.*, section 3.2. Thus, similarly to the relative cost of logic cones of Leaver, the rankings are not of input assignments. In particular, there is no mention of a number of times that a signal is assigned to a particular input of any type of hardware, fixed-configuration or otherwise. Accordingly, the combination also does not teach or suggest "*ranking the input assignments by determining a number of times each of a plurality of signals in the user design is assigned as a respective input to the fixed-configuration secondary hardware.*

For at least the reasons stated above, Applicant submits that claim 1 and its dependent claims 2-15 are allowable over the cited references.

Other claims

Claims 20 and 36 should be allowed for similar reasons as claim 1. The other claims depend on one of the above claims and should be allowed for at least the same reasons and for the additional limitations they recite.

Claim Rejections under 35 USC § 103(a), Leaver, Cong, Wallace

Claims 10-15 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. in view of Cong and in further view of Wallace (US Patent No. 7,020,855). These claims respectively depend upon allowable independent claims 1 and 20, and are thus allowable. Note that the cited teachings of Wallace fail to make up for the deficiencies in Leaver and Cong.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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